

WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

forming a buried layer of a semiconductor substrate;

5 forming an active region adjacent at least a portion of the buried layer;

forming an isolation structure adjacent at least a portion of the active region;

10 forming a gate oxide adjacent at least a portion of the active region;

forming a polysilicon layer adjacent at least a portion of the gate oxide;

15 removing at least a portion of the polysilicon layer to form a polysilicon definition structure, wherein the polysilicon definition structure at least substantially surrounds and defines an emitter contact region; and

forming an implant region of the emitter contact region, wherein the implant region is self-aligned.

20 2. The method of Claim 1, wherein removing at least a portion of the polysilicon layer to form a polysilicon definition structure comprises:

25 masking a first portion of the polysilicon layer, leaving a second portion of the polysilicon layer unmasked; and

removing the second portion of the polysilicon layer.

30 3. The method of Claim 1, further comprising forming an implant region of a base contact region, wherein the base contact region is proximate an outer edge of the polysilicon definition structure.

4. The method of Claim 1, wherein a width of the polysilicon definition structure is approximately 0.4 to 0.6 microns.

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5. The method of Claim 1, wherein a width of the emitter contact region is approximately 0.6 microns.

6. The method of Claim 1, wherein the isolation  
10 structure comprises a local oxidation on silicon (LOCOS)  
isolation structure.

7. The method of Claim 1, wherein the isolation  
structure comprises a shallow trench isolation (STI)  
15 structure.

8. The method of Claim 1, wherein the active region has a depth of approximately 3.5 microns.

9. The method of Claim 1, further comprising  
20 forming an emitter contact at the emitter contact region.

10. The method of Claim 1, further comprising  
forming one or more spacer structures adjacent the  
25 polysilicon definition structure.

11. The method of Claim 1, wherein the spacer structures comprise a nitride.

12. A semiconductor device, comprising:  
a buried layer of a semiconductor substrate;  
an active region adjacent at least a portion of the  
buried layer;

5 an isolation structure adjacent at least a portion  
of the active region;

a gate oxide adjacent at least a portion of the  
active region;

a polysilicon definition structure adjacent at least  
10 a portion of the gate oxide, wherein the polysilicon  
definition structure at least substantially surrounds and  
defines an emitter contact region; and

an implant region of the emitter contact region,  
wherein the implant region is self-aligned during  
15 formation.

13. The semiconductor device of Claim 12, further  
comprising an implant region of a base contact region,  
wherein the base contact region is proximate an outer  
20 edge of the polysilicon definition structure.

14. The semiconductor device of Claim 12, wherein a  
width of the polysilicon definition structure is  
approximately 0.4 to 0.6 microns.  
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15. The semiconductor device of Claim 12, wherein a  
width of the emitter contact region is approximately 0.6  
microns.

30 16. The semiconductor device of Claim 12, wherein  
the isolation structure comprises a local oxidation on  
silicon (LOCOS) isolation structure.

17. The semiconductor device of Claim 12, wherein the isolation structure comprises a shallow trench isolation (STI) structure.

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18. The semiconductor device of Claim 12, wherein the active region has a depth of approximately 3.5 microns.

10 19. The semiconductor device of Claim 12, further comprising an emitter contact at the emitter contact region.

15 20. The semiconductor device of Claim 12, further comprising one or more spacer structures adjacent the polysilicon definition structure.

21. The semiconductor device of Claim 12, wherein the spacer structures comprise a nitride.

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